REMARKS

Claims 1-6 are now pending in the application. Support for the amendments to the claims can be found throughout the drawings and specification. As such, no new matter is added. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102 AND 103

Claims 1-5 are rejected under 35 U.S.C. § 102(b) as being anticipated by Tsang et al. (U.S. Pat. No. 5,900,623). This rejection is respectfully traversed.

With respect to claim 5, Tsang fails to show, teach, or suggest applying a predetermined voltage to each gate of a plurality of the transistors from a first voltage source while in an accumulation state, and applying another predetermined voltage from a second voltage source to each gate of the plurality of transistors while in a reading out state.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. <u>Scripps Clinic & Res. Found. V. Genentech, Inc.</u>, 18 USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. <u>Constant v. Advanced Micro-Devices, Inc.</u>, 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Tsang fails to disclose the limitation of applying another predetermined voltage from a second voltage source to the gates of the plurality of the transistors while in a reading out state.

As shown in an exemplary embodiment in FIG. 2 of the present application, first and second voltage sources that are each coupled to the circuit for changing the gate-applied voltage. The circuit applies a first voltage from the first voltage source to gates of each of a plurality of transistors, and applies a second voltage from the second voltage source. In other words, during different periods, multiple voltage sources are applied to **the same gates**. More specifically, the first voltage source is applied to multiple gates during a first state and the second voltage source is applied to **the same** multiple gates during the second state.

As shown in FIG. 4 of Tsang, each transistor N1-N5 appears to always be connected to the same source during the accumulation state and the reading out state. In other words, N1 is always connected to SCB, and N2 is always connected to SC. In particular, none of the transistors are connected to different sources specifically during the two different states as claim 1 recites.

In response, the Examiner alleges that "the plurality of transistors do not have to be the same transistors, as interpreted by the examiner. They merely have to be contained in the same group of transistors." (See Page 3 of the Office Action mailed October 16, 2007). Applicant respectfully disagrees and submits that the Examiner's interpretation of Applicant's claim in view of Tsang is blatantly improper. When a term is introduced in a claim with an indefinite article and subsequently referred to with a definite article, the second reference inherently and implicitly refers to the same element previously introduced.

Claim 5 initially recites "each gate of the transistors." In other words, the voltage is applied to all of the gates of the transistors from the first source. Claim 5

subsequently recites applying the voltage to "each gate of the transistors." Neither these transistors nor their gates are introduced as a different group from the first recitation of "each gate of the transistors." Instead, "each gate" still refers to all of the gates of the same transistors previously introduced. As long as any element is preceded by a definite article such as "the," the only proper interpretation is that the term refers to the same exact element previously introduced. As such, Applicant asserts that the Examiner's allegation that the second recitation of "all of the gates of the transistors" does not have to be the "same transistors" is improper.

In view of the foregoing, Applicant respectfully submits that Tsang fails to disclose applying voltages to each of the gates of the transistors from both voltage sources in different states and, as such, claim 5 should be allowable for at least the above reasons. Applicant amended claims 1 and 6 to remove the limitation "at least one of." As such, claims 1 and 6, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner

believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: January 15, 2008

S. Gregory Sonivley

Bryant E. Wade Reg. No. 40,344

HARNESS, DICKEY & PIERCE, P.L.C. P.O. Box 828 Bloomfield Hills, Michigan 48303 (248) 641-1600

GGS/BEW/dms